REMARKS

In response to the Final Office Action dated January 31, 2008, claims 6-8, 11 and 15-16 are amended, claims 13-14 are cancelled without prejudice, and claim 17 is newly added. Claims 1-5 were previously cancelled without prejudice. Claims 6-12, and 15-17 are now active in this application. No new matter has been added. Claims 6, 15, and 16 are independent.

Applicants appreciate the indication of allowable subject matter in claims 15 and 16, which are objected to for depending from a rejected claim, and are allowable if rewritten in independent form including the limitations of their base claim and any intervening claims. Applicants submit that this objection has been overcome by the foregoing amendments, wherein claims 15 and 16 have been rewritten in independent form including the limitations of their base claim and any intervening claims.

Claims 6-9 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Shoji (U.S. 4,670,670). Applicants traverse this rejection.

Claims 13 and 14 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Kaenel et al. (U.S. 5,682,118). Applicants submit that this rejection is moot because these claims have been cancelled.

Claims 6-9 and 11 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Tang et al. (U.S. 2004/0070440) in view of Forbes et al. (U.S. 6,456,157). Applicants traverse this rejection.

Claims 10 and 12 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Tang in view of Forbes and further in view of Bowden (U.S. 4,427,935). Applicants traverse this rejection.

Independent claim 6 recites, in part:

> **a differential amplifier circuit comparing the voltage value generated by the current-voltage conversion circuit with the operating power supply voltage and outputting a voltage for controlling the substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the operating power supply voltage value of the main circuit...**

As is well known, anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). The elements must be arranged as required by the claim. *In re Bond*, 910 F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). At a minimum, the cited prior art reference does not disclose (expressly or inherently) or suggest the above recited highlighted (bolded) element.

The Office Action, at page 2, asserts that all of the elements of claim 6 are allegedly disclosed by FIG. 1 of Shoji. Shoji describes FIG. 1 at column 2, line 43 to column 3, line 2, stating:

> FIG. 1 shows a portion 10 of a CMOS VLSI system including representative MOS integrated circuit 11 (i.e., a CMOS chip) subject to threshold voltage variation because of, for example, exposure to γ-radiation. Circuit 11 includes an NFET 12 connected source to drain between a pad 13 and ground as shown. The gate electode of NFET 12 also is connected to pad 13. Pad 13 comprises an output of circuit 11. Power (V_{DD}) is supplied to an N-Tub area, coincident with the broken line indicating the boundary of circuit 11 and in which circuit 11 is formed.
>
> A feedback loop comprising operational amplifier (op-amp) 20 is provided to adjust for any variation in the threshold of FET 12. The output of op-amp 20 is connected to pad 21. Pad 21 also is connected to any other P-Tubs which might be formed within chip 11. The positive input of op-amp 20 is connected to pad 13 and to resistor 22 in order to provide information as to the conductivity of the NFET 12. In this connection, NFET 12 is maintained at a state between the conducting and the nonconducting state and resistor 22 has a value chosen to maintain NFET 12 in that "between" state. Any variation of NFET 12 from this between state results in a large change in conductivity which affects the positive input voltage of op-amp 20. NFET 12 thus functions as a reference transistor within chip 11.

However, claim 6 has been amended to clarify the structure of the differential amplifier circuit. Thus, at a minimum, Shoji does not teach or suggest, "**a differential amplifier circuit comparing the voltage value generated by the current-voltage conversion circuit with the operating power supply voltage and outputting a voltage for controlling the substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the operating power supply voltage value of the main circuit,**" as required by amended claim 6. Thus, Applicants submit that claim 6 is not anticipated by Shoji.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. Further, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). At a minimum, the cited prior art references do not disclose (expressly or inherently) or suggest the above recited highlighted (bolded) element.

The Office Action, at pages 6 and 7, asserts that the combination of Tang and Forbes discloses all of the elements of claim 6. Specifically, the Office Action, at page 7, asserts that element 102 in FIG. 1 of Tang discloses the differential amplifier element of claim 6. Tang describes element 102 at paragraph [0009], stating:

> [0009] Some embodiments are associated with circuits that generate a body bias voltage for application to one or more transistors. Details of features of embodiments will be described by first referring to FIG. 1 where a body bias circuit 100 is depicted. Body bias circuit 100 includes a **differential difference amplifier (DDA) 102 configured to receive a bias voltage (V_{bs}), a local supply voltage (V_{cc}) and a feedback signal 106 from the output ($V_{out'}$) of a buffer 104. Buffer 104 receives an output signal (V_{out}) from DDA 102.** The signal

> (V_{out}) output from buffer 104 is a body bias voltage that is distributed to one or more transistors 108. For example, in some embodiments V_{out} is distributed to a plurality of transistors of an integrated circuit. For clarity and ease of exposition, the transistor 108 of the circuit of FIG. 1 will be referred to in the singular; however, embodiments distribute V_{out} to a plurality of transistors as will be described further below in conjunction with FIGS. 3 and 4.

However, claim 6 has been amended to clarify the structure of the differential amplifier circuit. Thus, at a minimum, Tang does not teach or suggest, "**a differential amplifier circuit comparing the voltage value generated by the current-voltage conversion circuit with the operating power supply voltage and outputting a voltage for controlling the substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the operating power supply voltage value of the main circuit,**" as required by amended claim 6. Forbes also fails to disclose the foregoing element recited by amended claim 6.

Thus, at a minimum, the combination of Tang and Forbes fails to teach or suggest the foregoing element, and therefore Applicants submit that claim 6 is allowable over the cited art.

Further, Applicants submit that the other cited prior art does not remedy the deficiencies of Tang and Forbes. For example, Kaenel discloses a differential amplifier 105 in FIG. 7, but does not teach or suggest, "**a differential amplifier circuit comparing the voltage value generated by the current-voltage conversion circuit with the operating power supply voltage and outputting a voltage for controlling the substrate potential of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the operating power supply voltage value of the main circuit,**" as required by amended claim 6.

Under Federal Circuit guidelines, a dependent claim is allowable if the independent claim upon which it depends is allowable because all the limitations of the independent claim are

contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987).

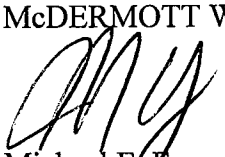
Thus, as independent claims 1 and 15 are allowable for the reasons set forth above, it is respectfully submitted that dependent claims 7-12 and 17 are allowable for at least the same reasons as their respective base claims.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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